End-to-end Verification with Portable Stimulus on a Mixed Signal DSP & Automotive SoC

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ANALOG DEVICES AHEAD OF WHAT'S POSSIBLE™

Motivation

Accellera Portable Stimulus Standard (PSS) ratified at DAC'18

- Promises reduced UVM/SoC test complexity, portability and test reuse

ADI evaluated PSS on two existing, complex testbenches

- Multi-core DSP SoC with an analog front-end
- Automotive mixed signal SoC

Some interesting methodology improvements

- VIP reuse from IP to SoC, across simulation, emulation, final silicon
- UVM sequence and SW tests complexity reduction
- Abstractions to allow non-verification experts to create test scenarios

Generalized Test Requirements

Test Generation Support

- IP and SOC level support
- Test authoring ease by non-DV engineers
- Layering into existing environments
- Initial bring up time and effort
- Test read-ability and ease of debug
- SystemVerilog and C Test support
- Speed of test generation
- Code/Functional Coverage of Generated Tests
- Generation of invalid tests

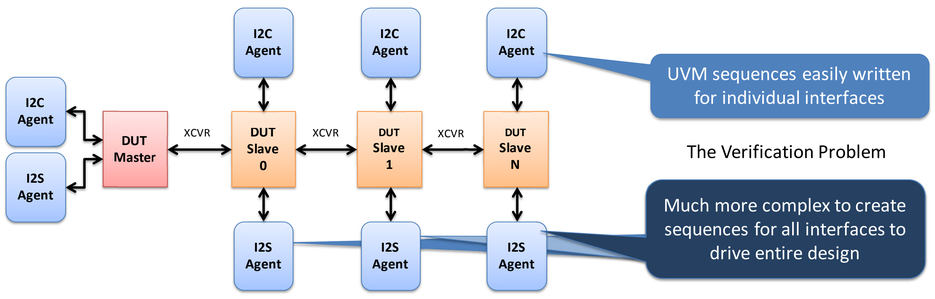
Re-use Requirements

- IP level to SOC level reuse
- Cross SoC platform reuse
- Post silicon driver development
- Derivative test regeneration/reuse

SOC Level Requirements

- Supports Cache Testing
- Supports Coherency Testing
- Control of UVM VIP virtual sequences
- Low power and security feature testing
- Advanced Testing of multi-core SoCs

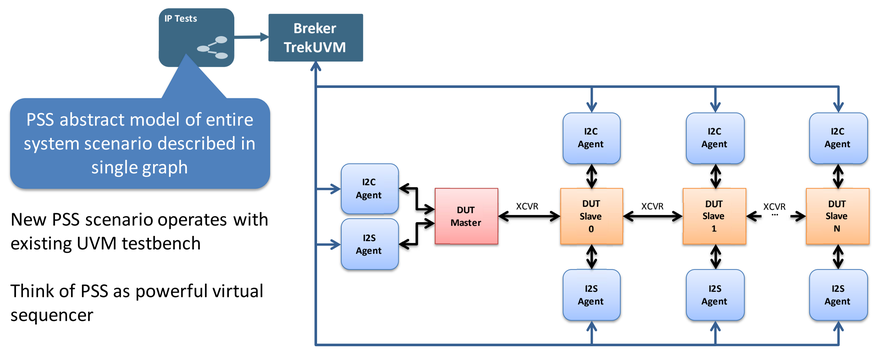
Mixed Signal, Automotive Audio SoC



Why is this an interesting testcase?

- Mixed signal elements modeled
- I2C & I2S interfaces modeled
- Very flexible design configuration leading to many possible tests
- Reusing existing UVM components

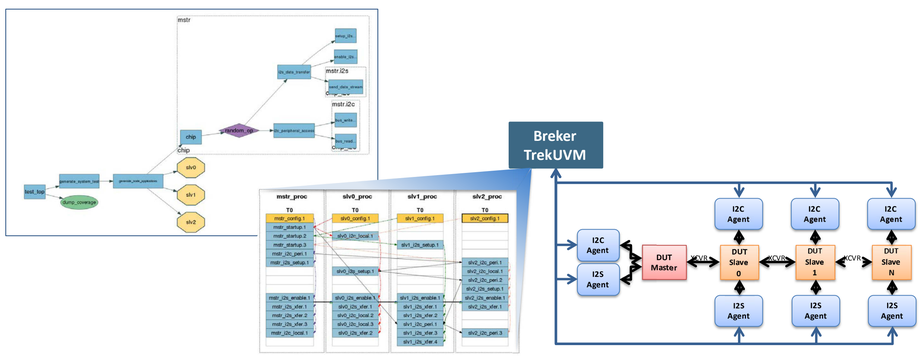
Single Abstract Scenario For Entire Design



New PSS scenario operates with existing UVM testbench

Think of PSS as powerful virtual sequencer

Automated, Multi-Threaded Sequence Synthesis

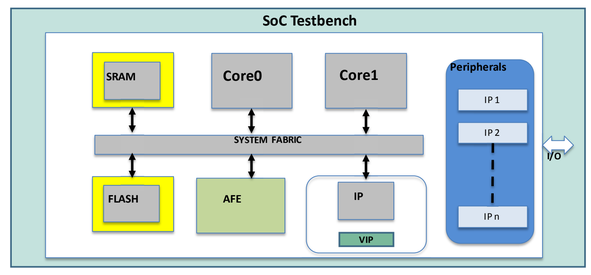


Sequences hard to generate manually given the synchronization complexity
Single scenario graph driving multi-threaded sequences simplifies this issue
Test map view makes test monitoring and design debug far easier

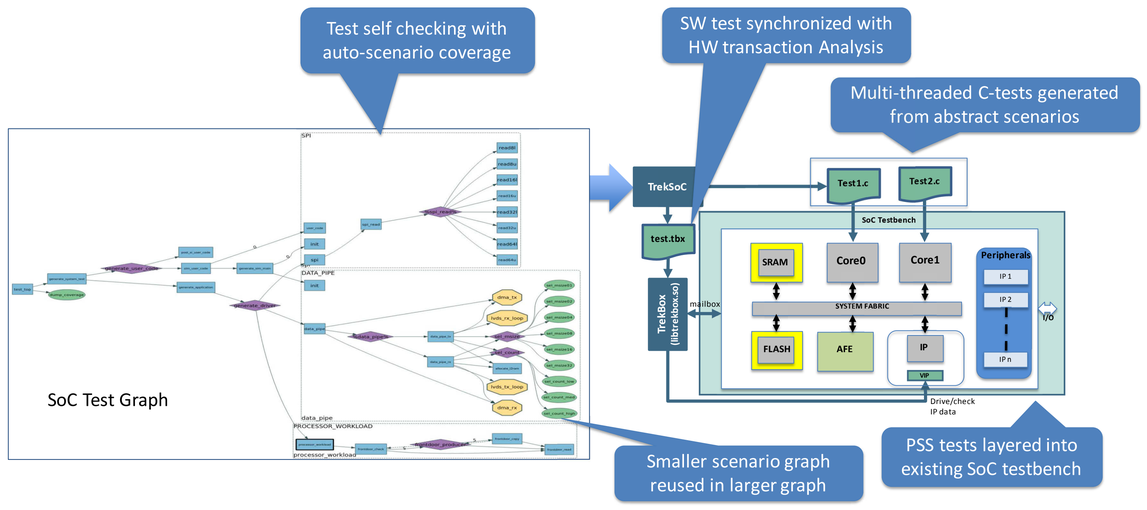
Dual Core DSP SoC with Analog Front-End

Verification challenges:

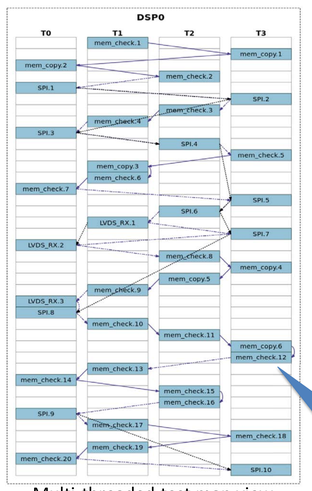
- Test case authoring by architects with limited verification expertize
- Synchronization of C-tests and HW transactions
- UVM model reuse at the SoC level
- Test case sharing from simulation to emulation and beyond

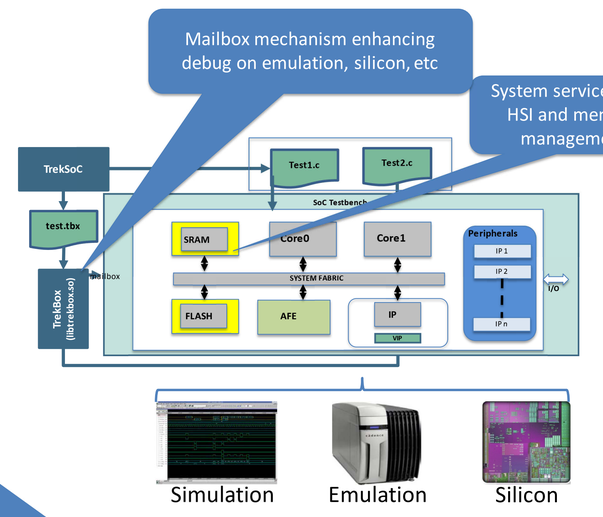


SoC Test Creation Advantages



SoC Test Execution Advantages





Summary of Interesting Findings

- Layer PSS effectively into existing UVM and SoC testbenches, use sequence generation based on abstract scenario models from non-verification engineers
- Effective methods to reuse IP simulation test scenarios within system level tests without rewriting, to drive SoC emulation and post-silicon verification
- Debug through mailbox mechanisms that monitors transactions. Particularly useful during post silicon where probing into the design impossible
- Complex random scenarios over the entire SoC provided powerful abstract tests, and coupled with coverage was able to enhance system analysis

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