BREKER SYSTEMVIP
SYSTEM COHERENCY™

Comprehensive System Coherency Verification

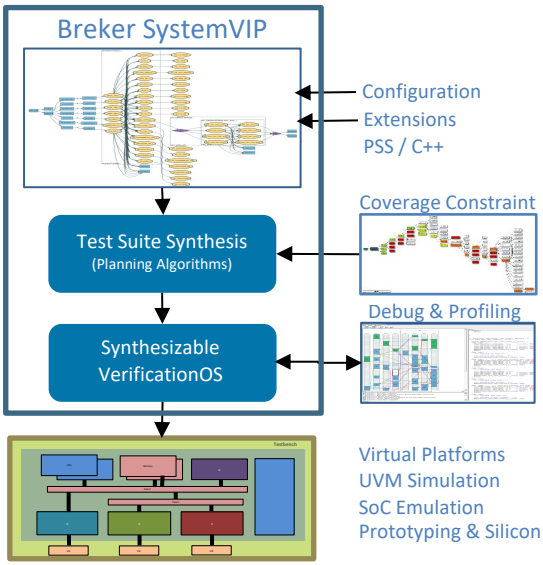
- **Broad range of public and proprietary algorithms to stress complex SoC coherency**
- **Easily configurable & extendable scenarios for a broad range of SoC platforms & processors**
- **Directly observe multi-threaded cache behavior and easily debug and profile system issues**

Elevating Coherency to the System Level

Breker's popular Cache Coherency SystemVIP, as used by most of the leading semiconductor companies worldwide, has found 100s of bugs over many complex SoCs. However, as the complexity of modern SoCs increases, so does the requirement for system level coherency that includes fabric and I/O, as well as advanced memory architectures. Breker's next generation System Coherency SystemVIP, leveraging Test Suite Synthesis, has been designed to address these emerging challenges far more effectively than zero abstraction templating and similar schemes.

The Breker System Coherency SystemVIP works with Breker's Test Suite Synthesis technology to generate a broad range of coherency tests based on multiple verification algorithms. It may be easily configured to operate on all memory and fabric architectures across multicore platforms, leveraging many types and numbers of processors and multiple coherent agents. The synthesis platform includes AI planning algorithms, cross combination and concurrent scheduling for high-coverage, and complex corner-case evaluation.

The SystemVIP can generate both C code and transactions for SoC testbenches, or UVM sequences for cache unit and sub-system simulation. It will operate on virtual prototype, simulation, emulation, FPGA prototyping and even actual silicon platforms, and includes full debug and profiling of the device under test on those platforms. Coverage requirements may be entered pre-test generation to provide as comprehensive a test as the execution medium will allow.



Modular SoC Verification Solutions for Arm, RISC-V and Other Cores

The System Coherency SystemVIP contains the ARMv8 and ARMv9 instruction sets, as well as the RISC-V Instruction Set Architecture (ISA), including additional custom instructions. This allows it to be easily configured to drive ARM and RISC-V SoCs and sub-systems. In addition, the SystemVIP may be easily configured to add instruction sets for other processors, and has been used with the X86 instruction set and others.

As part of the Breker SystemVIP library, the System Coherency SystemVIP is designed to be incorporated together to form comprehensive verification scenario platforms for specific purposes. For example, the System Coherency SystemVIP can be combined with the RISC-V or Arm SoC-Ready SystemVIP, Security SystemVIP, the Power Domain Management SystemVIP to ensure the correct operation of the SoC and the processor within.

System Coherency Capabilities

The System Coherency SystemVIP generates tests based on a range of typical and novel algorithms. The verification metrics covered by the SystemVIP include:

- Cache State Transitions
- Cache Line Sharing Cases
- Snoop / Probe Sources
- Load/Store Operation Size
- Load/Store Sources
- False Sharing Cases
- Crossing Cache Line Boundaries
- Capacity Eviction Cases
- Address Stride Patterns
- Memory Workloads
- Multiple Memory Regions
- Concurrent Scenarios

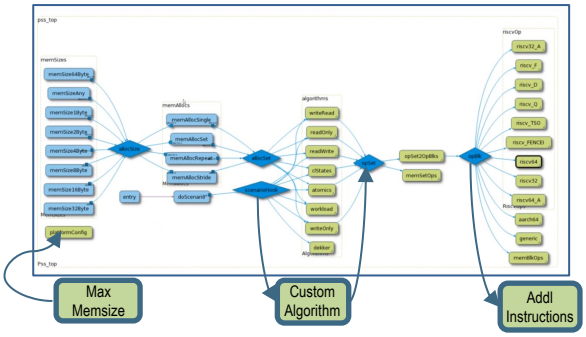
In addition, the SystemVIP also includes the following, more general processor integration scenarios:

- All Arm/RISC-V load/store instructions
- Memory Barriers / Ordering
- Randomized Interrupts
- Randomized Exception Level Switching
- Randomized WFE sleep / wakeup
- Page Table Randomization (TBA Q1'22)

The SystemVIP makes use of a variety of public and proprietary algorithms to accomplish the above metrics, including the Dekker Algorithm, Moesi State Analysis and many others.

Configurable, Extendable SystemVIP

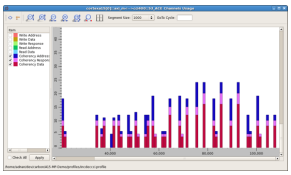
All the Breker SystemVIPs allow for universal configuration and extensibility to suit a variety of specialized test scenarios and applications. The System Coherency SystemVIP can be easily configured to drive a variety of processor instruction sets, including custom instructions, without changing test scenarios or using specialized languages. Custom test algorithms may also be added, and these will be amalgamated into the test generation process, multiplying the existing tests with the new.

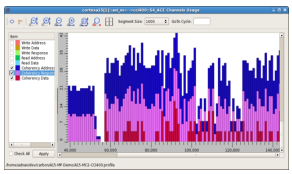


Coherency Results

Breker's Test Suite Synthesis has been shown to produce dramatic improvements in test composition time and coverage over and above basic test generators, including typical templating test schemes. System coherency is a notoriously complex and error prone task which requires considerable expertise and time to accomplish. By contrast, the System Coherency SystemVIP can be set up in a few days and will immediately generate high quality tests with minimal effort. The SystemVIP will create traffic with orders of magnitude increases in test density, driving high coverage execution and exercising hard-to-predict corner cases.

Manual Coherency Tests…





… vs Breker Coherency SystemVIP

BREKER™

Breker Verification Systems solves the challenges of functional verification for large, complex chips, including system-on-chip (SoC) designs containing one or more embedded processors.

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